FIG. 1

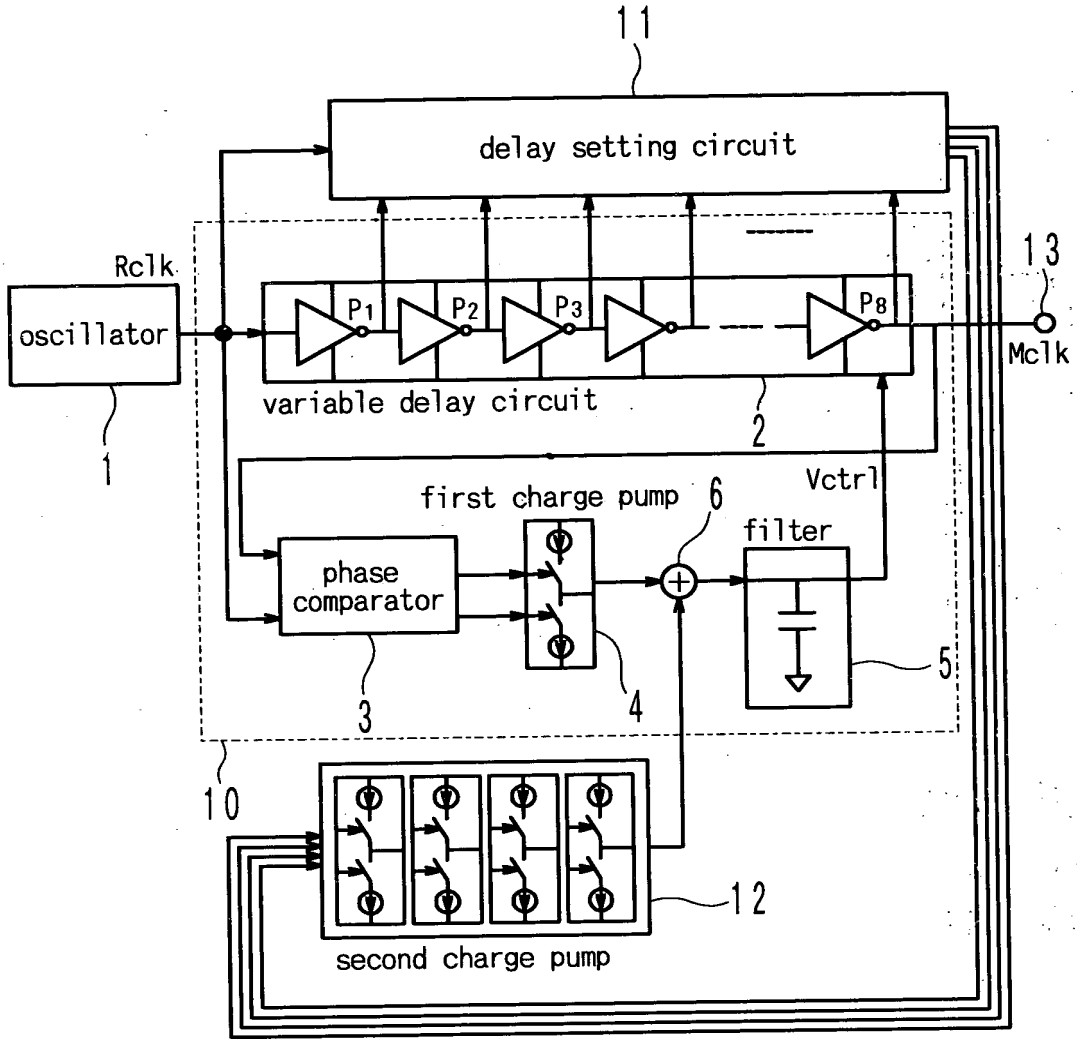

11
delay setting circuit
Rclk
oscillator
1
P1
P2
P3
P8
13
Mclk
variable delay circuit
2
Vctrl
first charge pump
6
filter
phase comparator
3
4
5
10
12
second charge pump

FIG. 2

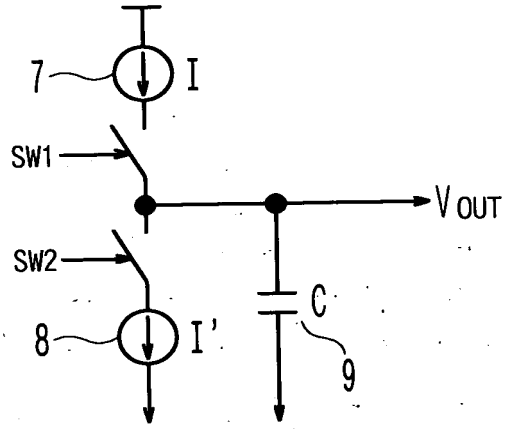

7
I
SW1
VOUT
SW2
C
8
I'
9

FIG. 3

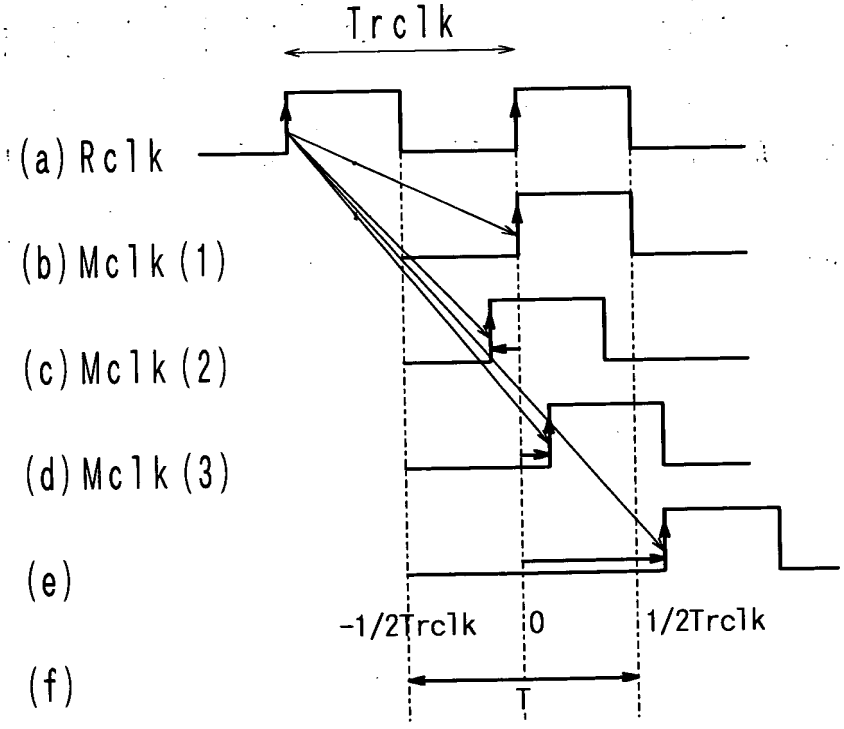

Trclk
(a) Rclk
(b) Mclk (1)
(c) Mclk (2)
(d) Mclk (3)
(e)
(f)
-1/2Trclk
0
1/2Trclk
T

FIG. 4

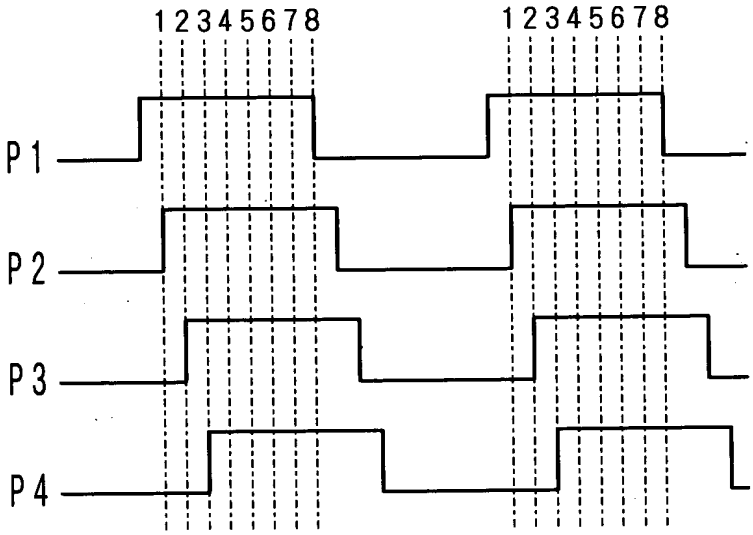


FIG. 5

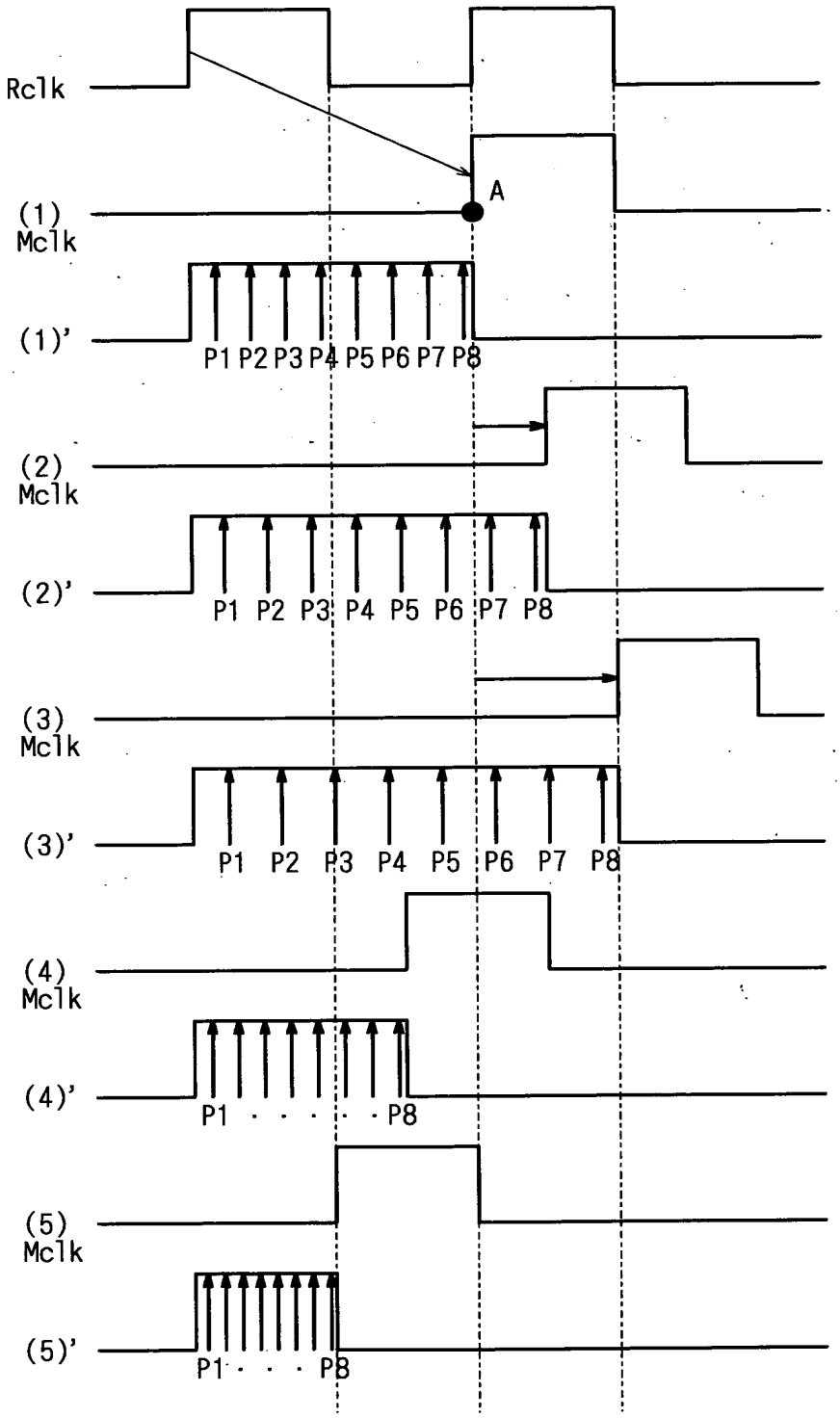

Rclk
A
(1)
Mclk
(1)'
P1 P2 P3 P4 P5 P6 P7 P8
(2)
Mclk
(2)'
P1 P2 P3 P4 P5 P6 P7 P8
(3)
Mclk
(3)'
P1 P2 P3 P4 P5 P6 P7 P8
(4)
Mclk
(4)'
P1 · · · · · · P8
(5)
Mclk
(5)'
P1 · · · P8

FIG. 6

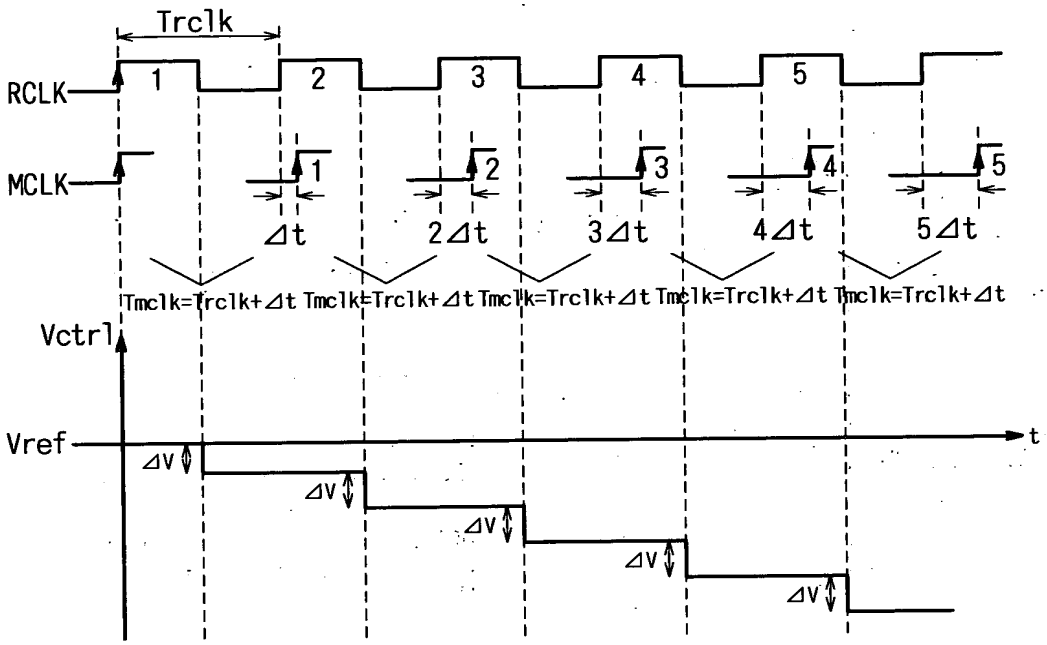
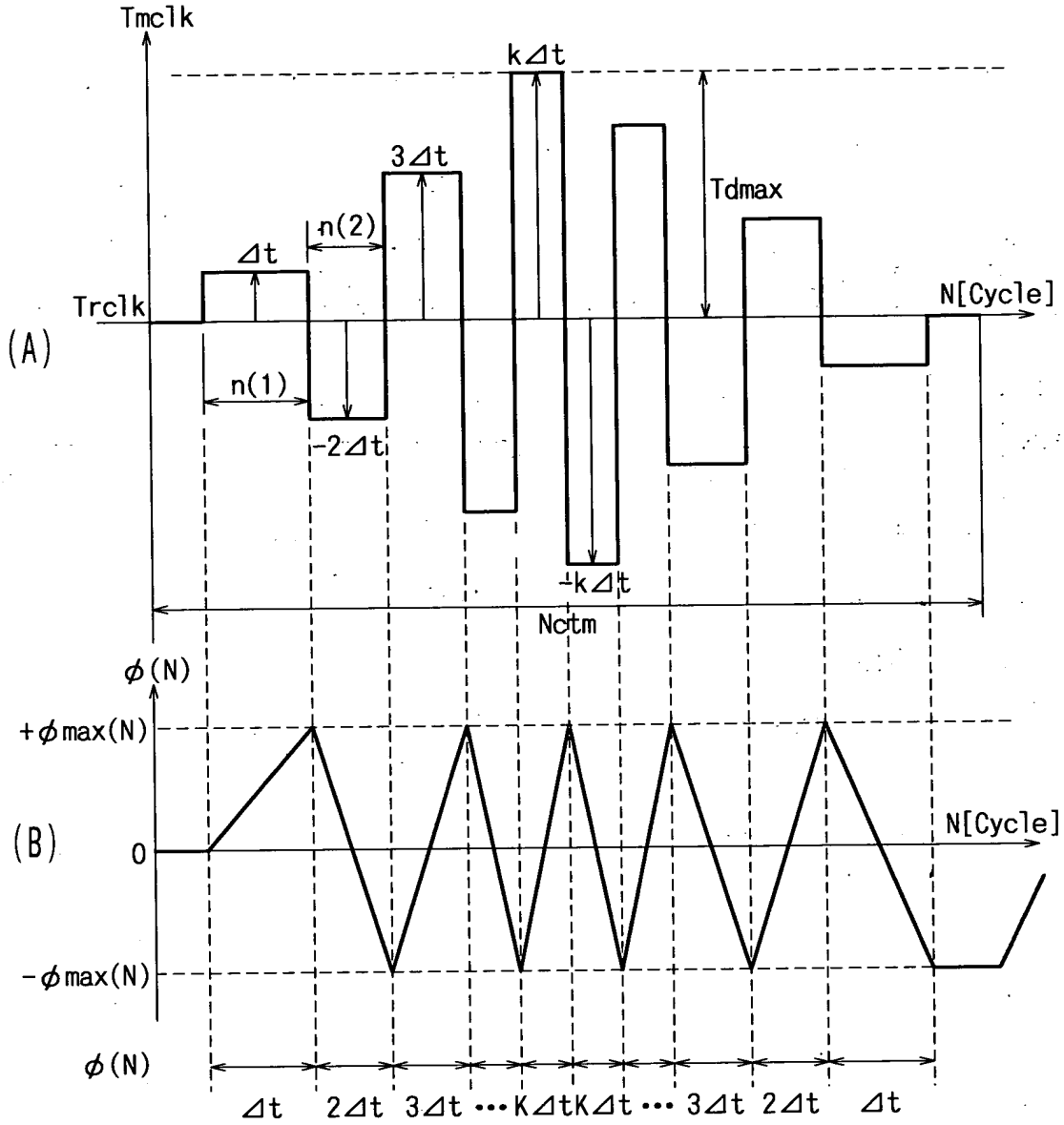

Trclk
RCLK
MCLK
1
2
3
4
5
⊿t
2⊿t
3⊿t
4⊿t
5⊿t
Tmclk=Trclk+⊿t Tmclk=Trclk+⊿t Tmclk=Trclk+⊿t Tmclk=Trclk+⊿t Tmclk=Trclk+⊿t
Vctrl
Vref
t
⊿V
⊿V
⊿V
⊿V
⊿V

FIG. 7



:phase difference
per one cycle

FIG. 8

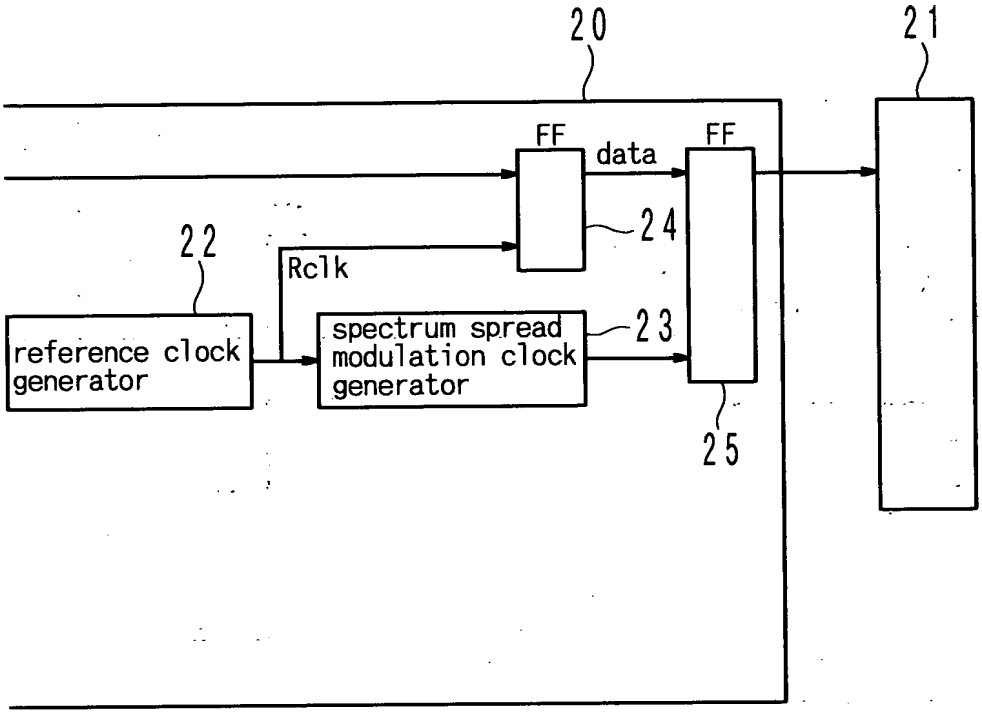
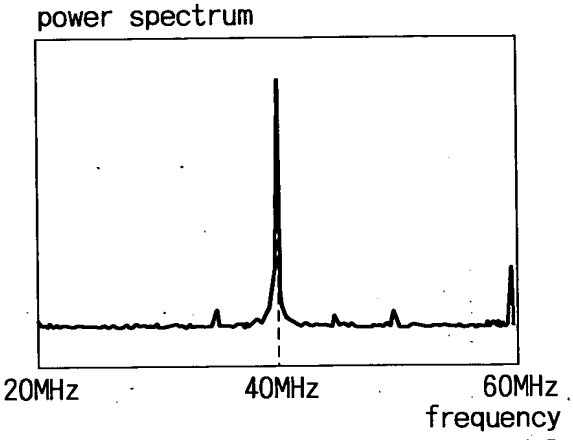

20
21
FF
data
FF
24
22
Rclk
reference clock generator
spectrum spread modulation clock generator
23
25

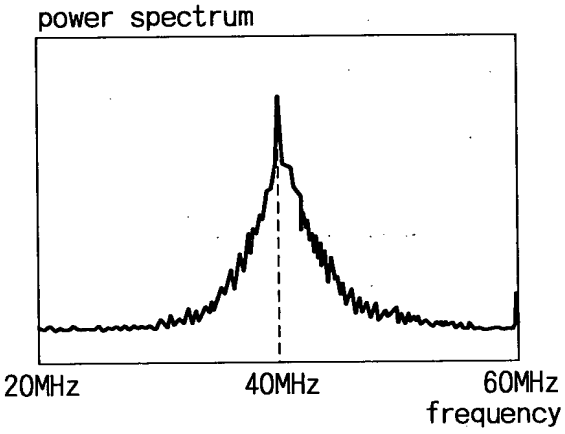
FIG. 9

(a)



Clock without spectrum spread modulation

(b)



Clock with spectrum spread modulation

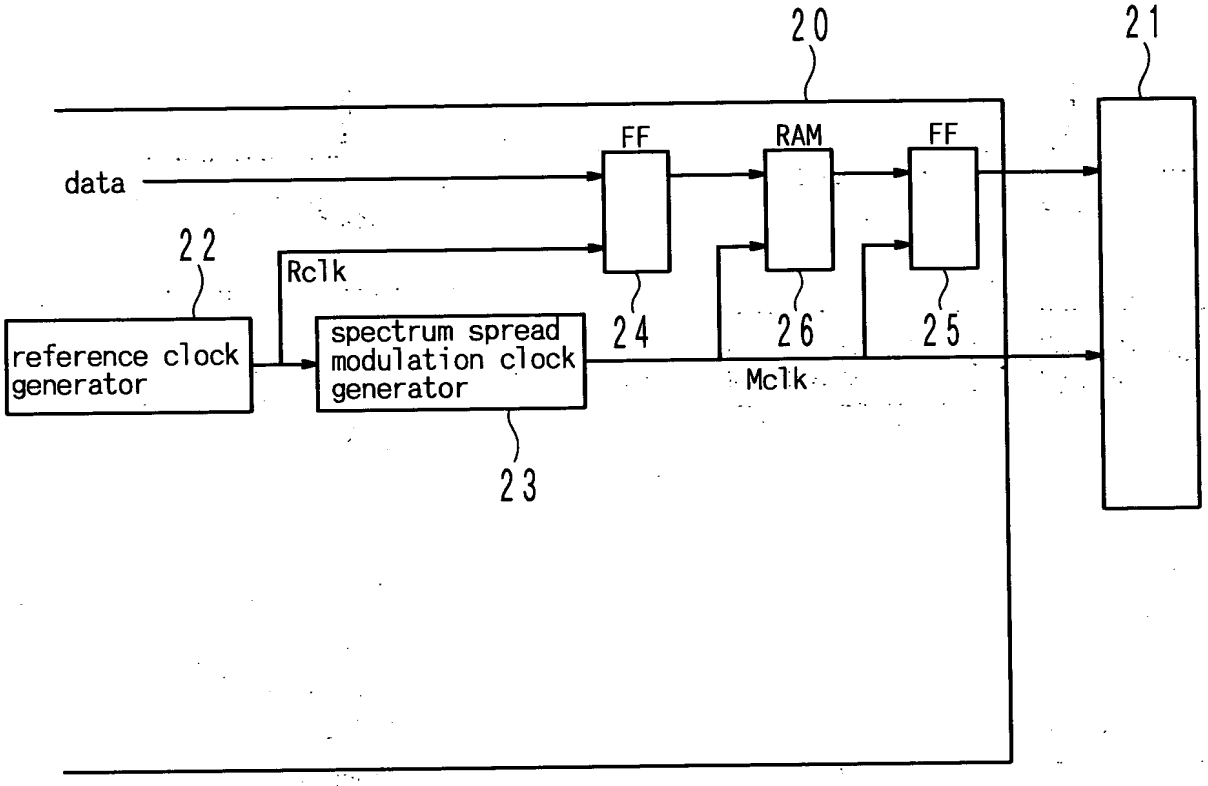



FIG. 10 (PRIOR ART)